AMENDMENTS TO THE SPECIFICATION

Please substitute the following replacement paragraphs for like-numbered paragraphs of the specification:

[0016] Still referring to Fig. 2, the check address generator 124 may be loaded to start error checking from a particular address within the CAM array. Also, the check address generator may be started from a known state, for example, upon device power-up or in response to a reset operation.

[0127] In one embodiment, each new check address 155 is compared with the contents of the error CAM array 800 regardless of the state of the error signal 712. Alternatively, comparison operations within the error CAM array 800 may be enabled only when the error signal 712 is asserted (i.e., check addresses for which the corresponding CAM word includes an error), for example, by selectively enabling a comparand driver circuit of the error CAM array 800 or by selectively asserting, via the instruction decoder or other control circuit, a control signal that enables the compare operation within the error CAM array 800. Also, in one embodiment, the read/write circuit 803 drives each new check address 155 onto write bit lines (WBL) of the error CAM array so that, if the load signal 950 is asserted, the corresponding row of the error CAM array will be enabled to store the check address 155. In an alternative embodiment, the load signal 950 may additionally be supplied to the read/write circuit 803, the read/write circuit 803 being enabled to drive a check address 155 onto the write bit lines of the error CAM array 800 only when the load signal 950 is asserted. Further, while the error CAM array 800 is depicted in Fig. 36 as a dual ported array (i.e., having separate write and read ports in the form of write bit lines, WBL, and read bit lines, RBL), the error CAM array 800 may alternatively be a single ported array in which read and write operations are multiplexed over time. For example, a single set of bit lines may be provided and used to read the error address 131 and error flag 132 from

the head entry of the error CAM array 800 whenever a load operation is not being performed. When a load operation is being performed, the read operation is temporarily suspended while the bit lines are used to store a new error address into the error CAM array 800. Additionally, the read operation within the error CAM 943 may be performed continuously (except during load operations) or only occasionally (e.g., in response to host read requests). For example, the error signal 712 may be output to a host processor (or other control device) via a status word or dedicated signaling line to signal each error detection event. The error signal 712 may be polled by the host or coupled to a host interrupt input to initiate host execution of an interrupt service routine to read an error address from the CAM device.

[0129] Fig. 38 illustrates an embodiment of a multi-ported CAM cell 960 that may be used to implement individual storage/compare elements within the error CAM array 955. The CAM cell 960 is similar to the CAM cell 801 described in reference to Fig. 30 except that the CAM cell 960 includes an additional comparand port to receive complementary comparand bits of the check address, C_{CA} and $\overline{C}_{CA}$, and an additional compare circuit 961 to compare the check address comparand (i.e., a constituent bit of check address 155 and its complement) to the content of the storage element 901. Note that the complementary bits of the index (i.e., index 174 of Fig. 37) are designated C_{IN} and $\overline{C}_{IN}$ in Fig. 38 to distinguish the index bits from the check address bits. The output of the compare circuit 961 is coupled to match line 946, while the output of compare circuit 910 is coupled to match line 827. In one embodiment, compare circuits 961 and 910 are both pull-down circuits (as shown, for example, by element 910 of Fig. 31) to pull an otherwise pulled-up match line to a low state to signal a mismatch condition. Other types of compare circuits may be used in alternative embodiments. Also, as discussed above, a single bit line may be coupled to the storage element 901 to provide a shared read/write

access port (i.e., instead of the separate read and write bit lines, RBL and WBL).